BROAD BAND MONOLITHIC CROSS POINT SWITCH MATRICES

Scott Powell, Paul Becker, Michael Dupuis, Christopher Nagy

Lockheed Sanders, Inc.
Microwave Technology Center
Nashua, NH 03061-2041

Abstract

A series of broadband monolithic switch matrices has been fabricated. Circuits covering DC to 18 GHz are described, including a 4 to 10 GHz fully monolithic 2 by 2 matrix on a single chip with 4 dB insertion loss and greater than 40 dB isolation. The circuits utilize a high isolation microstrip crossover.

Introduction

Switch matrices have typically been large and cumbersome components in microwave systems. This is due largely to the three dimensional structure of most switch matrix assemblies. Although monolithic circuits have helped somewhat by providing smaller switch elements, the resulting components still use three dimensional housings to provide isolation between the various signal paths.[1]

Full monolithic implementation of switch matrices offers the potential for a very small matrix, provided high enough isolation can be achieved on-chip. Recently, monolithic circuits have been developed that allow switch matrix functions to be accomplished on a single chip, including a full-access 2 by 2 matrix.[2,3] The greatest system functionality is achieved from a full-access matrix, where any combination of inputs can be connected to any combination of outputs, providing maximum flexibility in allocating system resources.

In order to realize large order matrices, (8 by 8 for example) the monolithic circuits should be easily cascadable. A matrix approach that allows cascading smaller matrices into larger ones is the cross bar, or cross point matrix [4]. In this topology, an arbitrary number of inputs, N, is connected to an arbitrary number of outputs, M, via NxM cross points as shown in figure 1. Each cross point is controlled individually, and only a fraction of the signal is extracted at each cross point, allowing successive cross points to access the input signal. This technique maintains full access capability in the cascaded matrix, though buffer amplifiers may be required to maintain amplitude tracking. The small size and two-dimensional feature of the matrix will allow significant reduction in the size and weight of microwave switch matrices.

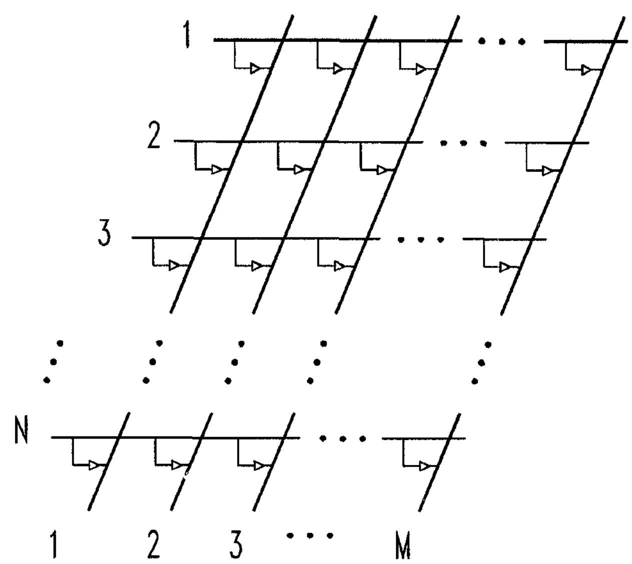

Figure 1. Block Diagram of Cross Point Matrix

Matrix Design

The matrix approach uses orthogonal input and output lines with an independent switching element at each cross point. Only a small percent of the input

IEEE 1990 Microwave and Millimeter-Wave Monolithic Circuits Symposium

signal is extracted at each cross point, so the input line can be continued on to drive additional cross points. The light coupling from the lines requires the cross points to provide gain to prevent excessive insertion loss in the matrix. The switching element uses dual gate FETs to provide both gain and isolation.

The method used to extract the RF signal from the input line is similar to a distributed amplifier, as the switching FET is absorbed into the input transmission line by using the parasitic capacitance of the gate (Cgs) to provide coupling from the input line to the transconductance of the FET. An inductor is used to absorb Cgs into an equivalent lumped transmission line, providing good return loss on the input line. The use of dual gate FETs is particularly well suited to this approach for several reasons: Cgs is smaller than that of a single gate FET, variations in the input impedance are small as the cross point is switched on and off, and isolation is high when the device is pinched off. Finally, the output of the FET can be connected directly to the output line using a short, high impedance transmission line since the drain has a high impedance and a small parasitic capacitance.

In order to provide high isolation, two dual gate FETs may be connected in series. A simple interstage matching network provides DC bias capability and slope equalization. A lumped-element low pass filter supplies drain bias to the second stage, while resistor networks provide bias to both gates. The two FET combination provides greater than 60 dB isolation for the active switch, so the overall matrix isolation is determined by the microstrip crossover. In the 2 by 2 matrix, the interstage matching at each cross point is slightly different to provide equal insertion loss through each path in the matrix.

Microstrip Crossover

The matrix topology requires on-wafer crossovers of microstrip lines at each cross point. In order to provide greater than 40 dB isolation on chip, a new microstrip airbridge crossover was developed. At the crossover the lines are reduced to 10 microns in width to minimize capacitance and add inductance. An additional layer of metalization (isolation plate) is placed between the two crossing lines, and is connected to ground with via holes to terminate the fields which would otherwise couple the two lines. The isolation plate is separated from the bottom microstrip line by dielectric, and the top microstrip line is airbridged over both. Without the isolation plate the crossover isolation is 35 dB at 6 GHz, and 30 dB at 12 GHz. With the isolation plate, isolation increases to 55 dB and 40 dB respectively.

MMIC Fabrication and Yield

All circuits were fabricated using Sanders standard 0.5 micron self-aligned N+ MMIC process. This process utilizes an N+/N structure formed by direct ion implantation of silicon into undoped GaAs. The gates are self-aligned through the N+ and the gate electrodes are formed by liftoff. Plasma deposited silicon nitride is used for thin film capacitors and for scratch protection of active devices. The standard MMIC process also provides N+/N resistors, electroplated gold transmission lines and air bridges, as well as plasma etched via holes through 125 micron substrates.

Circuit yields are important in a circuit as large as the 2 by 2 matrix (0.2 x 0.2 inch), especially with high MIM capacitance (85 pF) and FET periphery (4800 micron). Out of 3 wafer lots (18 wafers started), 16 wafers were completed through RF test. After 100% on-wafer testing (and before dicing) 16% of the available sites were DC and RF good.

Circuit Performance

Circuits built to date include a DC to 12 GHz cross point, a 6 to 18 GHz cross point, a 2 to 6 GHz 2 by 2 matrix, and a 4 to 10 GHz 2 by 2 matrix. All the circuits use a configuration that allows them to be cascaded into higher order matrices while maintaining full access capability. The monolithic crossover provides better than 40 dB isolation at 12 GHz between two crossing microstrip lines.

Several different circuits have been built and tested using this approach. A single cross point using a 300 micron periphery dual gate FET (figure 2) provides approximately 7 dB insertion loss and 30 dB isolation

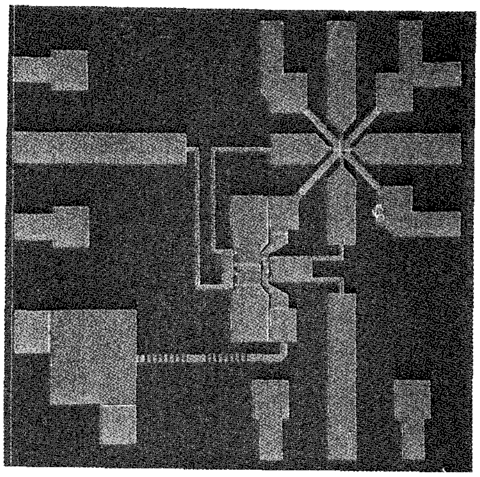

Figure 2. Photograph of DC - 12 GHz Cross Point.

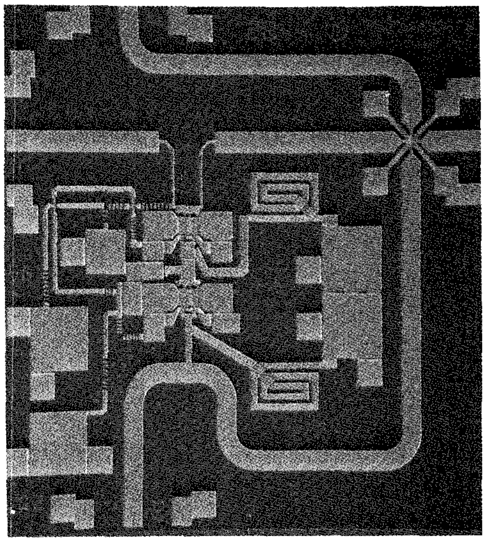

Figure 3. Photograph of 6 - 18 GHz Cross Point.

from DC to 12 GHz, with less than 2.0:1 VSWR. A second cross point (figure 3) was designed for the 6 to 18 GHz band. This circuit uses 2 FETs in series, and provides insertion loss of 5 to 10 dB with greater than 40 dB isolation from 6 to 18 GHz.

Several 2 by 2 matrices have been built as well; the results of a 6 to 10 GHz matrix will be described. The 6 to 10 GHz 2 by 2 matrix (figure 4) uses two 300

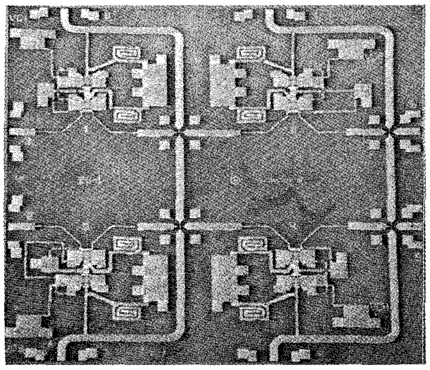

Figure 4. Photograph of 6 - 10 GHz 2 by 2 Matrix Chip.

micron periphery dual gate FETs with 0.5 micron gate length. In the "on" state they are biased at one-half Idss, with -1V on gate 1 and 0V on gate 2 (the control gate). Performance of the 2 by 2 monolithic matrix is shown in figures 5 through 7. The insertion loss through the matrix is approximately 4 dB, with 40 dB of isolation. The input VSWR under all conditions is better than 1.8:1, and the output VSWR is better than 2.2:1. The variation in insertion loss of a given path, as another is turned on or off, is very small - on the order of 0.2 dB. This data was taken on-wafer, using an automatic wafer prober and an HP8510 network analyzer. Since the chip has eight RF ports, multiple passes over the wafer were required to obtain the data.

When all cross points are turned off, the matrix consumes no DC power. For each cross point that is turned on, about 45 mA of DC current is drawn from the +5V drain supply. The insertion loss of the straight through input and output lines is important when cascading the circuit into higher order matrices. Insertion loss of each line is less than 3 dB up to 10 GHz. When these MMICs are cascaded into larger matrices, monolithic buffer amplifiers have been placed between the chips to provide a small amount of gain and eliminate VSWR effects.

Most recently, a 2 to 6 GHz 2 by 2 matrix using the same approach has been built and tested. This design uses two 600 micron dual gate FETs in series, and provides zero dB insertion loss over the 2 to 6 GHz band.

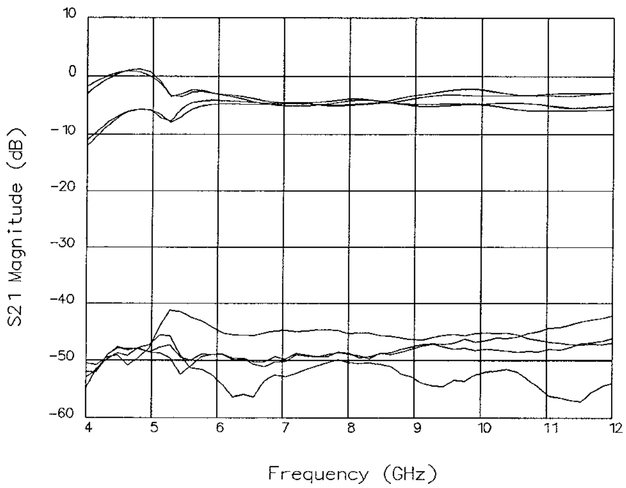

Figure 5. Insertion Loss and Isolation of Four Paths on 2 by 2 Matrix

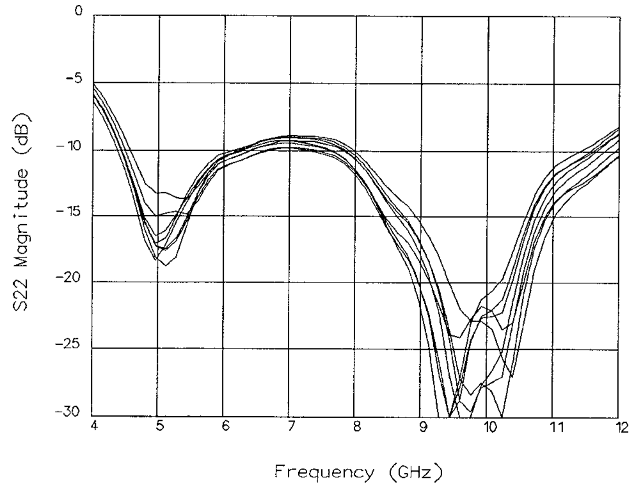

Figure 7. Output Return Loss of 2 by 2 Matrix

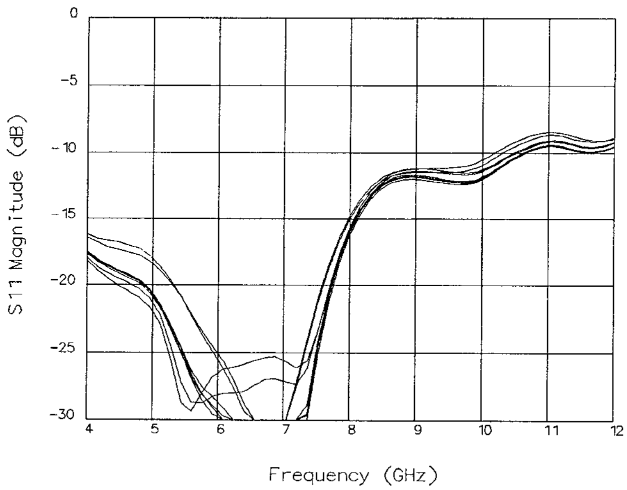

Figure 6. Input Return Loss of 2 by 2 Matrix

Conclusion

A series of broad band monolithic switch matrices operating from DC to 18 GHz have been built and tested, including a single chip 2 by 2 matrix operating over the 6 to 10 GHz range. The circuit includes on-chip microstrip crossovers, and provides greater than 40 dB isolation with 4 dB insertion loss. The chips can be cascaded to form higher order matrices.

Acknowlegdements

This work was funded in part by the Naval Ocean Systems Center, under Contract No. N6601-87-C-1089. The authors would like to acknowledge Eric Knuth, John Reindel, Miles Goff, Paul Bernkopf, and the entire staff of the Microelectronics Center for their important contributions to this work.

References

[1] R. Gupta, H. Gerson, P. Ross, F. Assal, "Design and Packaging Approach for MMIC Insertion in a Broadband 4 X 4 Switch Matrix," GaAs IC Symposium Technical Digest, November 1988, pp. 261-264.

[2] M. Schindler, and K. Simon, "A 2-18 GHz Non-blocking Active 2 X 2 Switch," GaAs IC Symposium Technical Digest, October 1989, pp. 181-183.

[3] M. Schindler, M. Miller, and K. Simon, "DC-20 GHz N X M Passive Switches," IEEE MTT-S Symposium Digest, May 1988, pp. 1001-1005.

[4] P. Ho, R. Pelose, and R. Maliszewski, "Coupler Crossbar Microwave Switch Matrix," IEEE MTT-S Symposium Digest, June 1982, pp. 239-241.